REMARKS

Claims 1-15 are present in this application. Claim 15 is new. Claims 1, 3, 5, and 8 are currently independent.

Allowed Claims

Applicant thanks the Examiner for indicating that claims 3, 4, 6, 7, 9, and 12 are allowed.

Claim Rejection – 35 USC 102

Claims 1, 2, 5, 8, 10, 11, 13, and 14 have been rejected under 35 U.S.C. 103(e) as being anticipated by Tajima et al. (U.S. Patent 6,373,911). Applicant respectfully traverses this rejection.

Claim 1 (e.g., Figure 8) is directed to a bit synchronizing circuit comprising a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to the input clock, and a clock selecting circuit having two inputs, one from the polyphase clock generation circuit and a detection result from the detection circuit, and produces one output, a selected polyphase clock.

The Office Action states that the phase comparison circuit of Tajima teaches the claimed detection circuit. However, unlike the

claimed detection circuit, Tajima's phase comparison circuit performs phase comparison of input data (e.g., receiving data) and polyphase clocks in order to determine phase comparison results (column 4, lines 45-51). In contrast, the present invention detects phase shift of the clock by comparing an input clock signal to delayed clock signals. Thus, at least for this reason, Applicant submits that Tajima fails to teach at least the claimed detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to the input clock.

Further, with respect to claim 5, the Office Action states that the holding circuit 8 of Tajima teaches the claimed operational circuit. The operational circuit of claim 5 samples an output from the detection circuit a plurality of times and carries out operations on sampled values. Unlike the present invention, Tajima's holding circuit 8 holds the result of phase determination when the frame clock becomes H (see column 6, lines 26-32); i.e., holds an output phase for clock determination during a period receiving one frame of input data. In the present invention, by sampling an output of the detection circuit a plurality of times, unstable operation is suppressed (see page 22, first full paragraph). Thus, at least for this reason, as well as reasons set forth above for claim 1, Applicant

submits that Tajima fails to teach at least the claimed operational circuit for sampling an output from the detection circuit a plurality of times.

Further, with respect to claim 8, the Office Action states that the decision circuit 4 of Tajima teaches the claimed bit synchronization working circuits. Claim 8 (e.g., Figure 7) recites a plurality of bit synchronous working circuits to which a polyphase clock is inputted from the polyphase clock generation circuit so that a bit synchronization operation is carried out at each different phase (see also paragraph bridging pages 24 to 25). Thus, unlike the flip-flops in the decision circuit 4 of Tajima, the present invention comprises a plurality of bit synchronous working circuits. Thus, at least for this reason, as well as the reasons set forth above for claim 1, Applicant submits that Tajima fails to teach each and every element of claim 8.

The same argument applies as well to the respective dependent claims. Accordingly, Applicant respectively requests that the rejection be withdrawn.

CONCLUSION

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and such allowance is respectfully solicited. Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No. 48,222), to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any

overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1. 17; particularly, extension of time fees.

Respectfully submitted,

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